

1.(Amended) A system comprising:

a bus;

a resource coupled to the bus; and

a plurality of entities coupled to the bus, at least one entity among the plurality of entities including a memory, wherein at least a portion of the memory of the at least one entity is selectively reset when the at least one entity has access to the resource, wherein the memory portion is reset if the entity does not currently have control of the resource, and wherein the memory portion is not reset when the at least one entity currently has control of the resource.

8.(Amended) An integrated circuit for allowing [at least one] a resource to be controlled by [a processor among] a plurality of processors including a first and second processor, wherein the first [at least one] processor [among the plurality of processors including] includes a fast memory, the integrated circuit comprising:

a bus;

a central computing unit coupled to the bus; and

a switch mechanism, coupled to the central computing unit, to switch the control of the [at least one] resource, wherein a portion of the fast memory of [at least one] the first processor [of the plurality of processors] is [selectively] reset when the control of the [at least one] resource is switched to the second processor and not reset when control of the resource remains with the first processor.

20.(Amended) An integrated circuit for allowing [at least one] a resource to be shared by [among] a plurality of processors, including a first and second processor, wherein the first [at least one] processor [among the plurality of processors including] includes a fast memory, the integrated circuit comprising:

a bus;

a central computing unit coupled to the bus; and

a lock coupled to the central computing unit to reserve exclusive control of the [at least

one] resource [to a processor among the plurality of processors], wherein [at least] a portion of the fast memory of the first processor [of the plurality of processors] is [selectively] reset when the second processor [of the plurality of processors] obtains [has] exclusive control of the [at least one] resource from the first processor and not reset when exclusive control remains with the first processor.

30.(Amended) A data structure in a machine-readable medium for allowing [at least one] a resource to be shared among a plurality of processors, at least one processor of the plurality of processors including a fast memory, the data structure comprising:

- a state for indicating that the [at least one] resource is under control; and
- a first identifier for identifying a past processor that had exclusive control of the [at least one] resource.

35. (Amended) The data structure of claim 30, further comprising a data type that is adapted to represent at least one portion of the [at least one] resource, wherein the data type includes at least one location of the at least one portion of the [at least one] resource and at least one dimension of the at least one portion of the [at least one] resource.

36.(Amended) The data structure of claim 30, further comprising a list that includes at least one location of at least one portion of the [at least one] resource and at least one dimension of at least one portion of the [at least one] resource.

37.(Amended) A method for allowing at least one resource to be shared among a plurality of processors, the method comprising:

- obtaining exclusive control over the at least one resource by a present processor, the present processor including a fast memory;

- identifying a past processor to obtain a first identity, wherein the past processor had exclusive control over the at least one resource; [and]

- identifying a present processor to obtain a second identity, the present processor having

exclusive control over the at least one resource;

comparing the first identity and the second identity so as to determine if the present processor is different from the past processor; and

resetting [selectively at least] a portion of the fast memory of the present processor when the past processor is different from the present processor and not resetting a portion of the fast memory of the present processor when the past processor is the same as the present processor.

42.(Amended) A method for scheduling access to a [at least one] resource from among a plurality of processors, the method comprising:

obtaining access to the [at least one] resource by [from] a requesting processor, the requesting processor including a cache memory;

excluding access to the [at least one] resource from the plurality of processors except for the requesting processor; and

resetting [at least] a portion of the cache memory of the requesting processor when the requesting processor is different from a processor that previously had access to the [at least one] resource, and not resetting a portion of the cache memory of the requesting processor when the requesting processor is the same as a processor that previously had access to the resource.

43.(Amended) An integrated circuit for allowing a [at least one] resource to be controlled by [a processor among] a plurality of processors, including a first and second processor, wherein the first [at least one] processor [among the plurality of processors including] includes a fast memory, the integrated circuit comprising:

a bus;

a central computing unit coupled to the bus;

a switch mechanism for switching the control of the [at least one] resource; and

a lock, in a cooperative relationship with the switching mechanism, for reserving exclusive control of the [at least one] resource to [a] the first processor [among the plurality of processors], wherein at least a portion of the fast memory of the first processor [of the plurality of processors] is [selectively] reset when the second processor [of the plurality of processors]

obtains [has] exclusive control of the [at least one] resource and not reset when the exclusive control of the resource remains with the first processor.

49.(Amended) An integrated circuit for allowing a [at least one] resource to be controlled by a [processor among a] plurality of processors, including a first and second processor, wherein the first [at least one] processor [among the plurality of processors including] includes a fast memory, the integrated circuit comprising:

a bus;

a central computing unit coupled to the bus; and

a scheduler, coupled to the central computing unit, for scheduling the control of the [at least one] resource, wherein a portion of the fast memory of the first [at least one] processor [of the plurality of processors] is [selectively] reset when the [at least one] resource becomes [is] under the control of the second processor and not reset when the resource remains under the control of the first processor.

52.(Amended) A system comprising:

a bus;

a [at least one] resource coupled to the bus;

a plurality of processors coupled to the bus including a first and second processor, wherein the first [at least one] processor [among the plurality of processors including] includes a fast memory; and

a switch mechanism, coupled to the bus, to switch the control of the [at least one] resource, wherein a portion of the fast memory of the first [at least one] processor [of the plurality of processors] is [selectively] reset when the control of the [at least one] resource is switched to the second processor and not reset when control of the resource remains with the first processor.

64.(Amended) A system comprising:

a bus;

a [at least one] resource coupled to the bus;

a plurality of processors coupled to the bus including a first and second processor,

wherein the first [at least one] processor [among the plurality of processors including] includes a fast memory; and

a lock to reserve exclusive control of the [at least one] resource [to a processor among the plurality of processors], wherein [at least] a portion of the fast memory of the first processor [of the plurality of processors] is [selectively] reset when the second processor of the plurality of processors obtains [has] exclusive control of the [at least one] resource from the first processor and not reset when exclusive control of the resource remains with the first processor.

74.(Amended) A system comprising:

a bus;

a [at least one] resource coupled to the bus;

a plurality of processors coupled to the bus including a first and second processor,

wherein the first [at least one] processor [among the plurality of processors including] includes a fast memory;

a switch mechanism to switch the control of the [at least one] resource; and

a lock, in a cooperative relationship with the switching mechanism, to reserve exclusive control of the [at least one] resource to a first processor [among the plurality of processors], wherein at least a portion of the fast memory of the first processor [of the plurality of processors] is [selectively] reset when the second processor [of the plurality of processors] obtains [has] exclusive control of the [at least one] resource and not reset when the exclusive control of the resource remains with the first processor.